Student assignment

Type: Graduation assignment
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Topic: investigation of deep learning optimizations for a coarse grained reconfigurable architecture.

Background:
At the electronic systems group we developed a very low-energy reconfigurable processor called Blocks. This processor outperforms a traditional microcontroller in performance with up to two orders of magnitude and typically uses approximately an order of magnitude lower energy to execute an application. Blocks achieves this by reconfiguring its hardware at runtime to match the properties of the application. If the application contains a lot of data parallelism then Blocks will be configured to form a vector processor, if there is instruction level parallelism then Blocks will form a VLIW processor. Anything in between, or even very application dependent structures (e.g. FFT or reduction trees) are also possible. By doing this cycles and memory accesses can be reduced significantly, leading to a much lower energy.

The switchboxes that allow Blocks to connect instruction decoders and functional units together are an important part of the system. Up till now however, relatively simple switchbox designs have been used. Our estimations show that we can reduce the overhead caused by these switchboxes with a significant amount (40% in area for example). This goal of this project is to develop energy efficient, area efficient and yet well performing switchboxes for Blocks. In this project you will:

- Investigate the state of the art in switchboxes on CGRAs and FPGAs.
- Determine how the switchboxes can be improved with respect to power, area and delay.
- Investigate improvements to the state of the art of switchboxes in CGRAs by using the architectural properties of Blocks.
- Implement the most promising option(s) and verify your estimations.

If you are interested in this assignment, or have some questions, please come around to have a chat.