NMC-general purpose simulator on FPGA  
Stefano Corda, s.corda@tue.nl, Eindhoven University of Technology, The Netherlands

“The conventional approach of moving data to the CPU for computation has become a significant performance bottleneck for emerging scale-out data-intensive applications due to their limited data reuse. At the same time, the advancement in 3D integration technologies has made the decade-old concept of coupling compute units close to the memory called near-memory-computing (NMC) more viable. Processing right at the “home” of data can significantly diminish the data movement problem of data-intensive applications” [1, 2]. This project aims at developing an NMC simulator on FPGA. While a fair amount of work has been spent on building NMC simulators [3], FPGA technology improved quickly. Furthermore, the new generation of Xilinx Alveo FPGAs, e.g. U50, are equipped with HBM. The main goal of this project is to develop a real NMC-general purpose simulator on FPGA, which can give more information quicker and more reliable than current state-of-the-art simulator.

Goal of this project and tasks:

- Study of cores (e.g. risc V) RTL models.
- Integration of the cores on FPGA.
- Validation and comparison with state-of-the-art simulators (e.g. Ramulator).

Skills acquired in this project
- Hands-on experience on FPGA programming.

Pre-requisite:
- C/C++.
- Verilog/VHDL/HLS.

Helpfull Skills
- Xilinx Vitis, Vivado.
- Work independently.

References