Design and implementation of a high performance asynchronous Network on Chip to be used in a GALS (globally Asynchronous Locally Synchronous) neuromorphic processor

Supervisor
Henk Corporaal

Contact person
Amirreza Yousefzadeh (ayousefzadeh@graimatterlabs.ai), Henk Corporaal (h.corporaal@tue.nl)

Problem definition of the thesis
GRAI MATTER LABS is a neuromorphic company dedicated to delivering low power processors for bio-inspired signal processing on the edge. The architecture is based on 2D array of basic computing units (neurons). These computing units are connected together using conventional communication architecture (synchronous network on-chip). As number of processing cores in the chip increases, main performance bottlenecks are due communication overhead.

In biology, communication between different cores are arranged in hierarchical, asynchronous manner. There is denser local-connectivity in time-aligned manner, while global connectivity is asynchronous. Based on the above, the proposed research focuses on applying GALS approach to study and build a communication infrastructure for the computing fabric. The study involves benchmarking the current approach against the new proposal. Consequently, a simulation model and scalable hardware implementation framework is desired outcome.

This project is aimed to design an asynchronous Network of GrAI-One cores on a chips which satisfy the latency/bandwidth requirement for the target applications.


Objective of the thesis
The master thesis would consist of the following activities:

- Became familiar with GrAI-One neuromorphic processors.
- Design space Exploration for asynchronous NoCs
- Design and simulate an asynchronous NoC and measure performance indexes
- Implementation of the NoC in HDL and the corresponding testbenches

Required Skills
Must have:
- Master student with electrical/computer engineering background
- Available for a period of 9-12 months
- Strong in digital design and RTL development (Verilog or VHDL)
- Strong in one of SystemC, C++, Python, MATLAB or OCaml.

Good to have:
- Basic knowledge in asynchronous design and Network on Chip
- Basic knowledge of bio-inspired event-driven processing

Location
GraiMatterLabs, HTC 65