Student assignment

**Type:** Graduation assignment

**Contact:** Mark Wijtvliet (m.wijtvliet@tue.nl)

**Topic:** investigation of deep learning optimizations for a coarse grained reconfigurable architecture.

**Background:**
At the electronic systems group we developed a very low-energy reconfigurable processor called Blocks. This processor outperforms a traditional microcontroller in performance with up to two orders of magnitude and typically uses approximately an order of magnitude lower energy to execute an application. Blocks achieves this by reconfiguring its hardware at runtime to match the properties of the application. If the application contains a lot of data parallelism then Blocks will be configured to form a vector processor, if there is instruction level parallelism then Blocks will form a VLIW processor. Anything in between, or even very application dependent structures (e.g. FFT or reduction trees) are also possible. By doing this cycles and memory accesses can be reduced significantly, leading to a much lower energy.

Deep learning has become a major source of interest and research. The algorithms used to perform deep learning have special properties which may or may not fit well with the Blocks architecture. The goal of this project is to investigate how Blocks can be optimized for these kind of algorithms. During this project you will:

- Investigate the state of the art in deep learning on CGRAs.
- Determine how deep learning can be efficiently applied to Blocks.
- Investigate improvements to the state of the art of deep learning on CGRAs by using the architectural properties of Blocks.
- Implement the most promising option(s) and verify your estimations.

If you are interested in this assignment, or have some questions, please come around to have a chat.