Code-generation for Flexible Reconfigurable Architectures

**Type:** MSc Graduation Assignment  
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**Background**

Coarse-grained reconfigurable architectures (CGRA) and other exposed datapath architectures such as transport-triggered architectures come with a high energy efficiency promise for accelerating data-oriented workloads. Their main drawback results from the push of complexity from the architecture to the programmer; compiler techniques that allow starting from a higher-level programming language and generate code efficiently to such architectures robustly is still an open research area.

We are actively working on an in-house compiler for the state-of-art Blocks Coarse-Grained-Configurable Array (CGRA), and looking for highly motivated students to take ownership of some of the research/development activities in this project. Specifically, we would like to investigate optimization strategies for energy-efficiency in the backend stages of our LLVM based compiler.

![Blocks CGRA Diagram](image)

**Task Description**

In this MSc thesis project, you are tasked to investigate, implement, and evaluate potential compiler optimization that improves code generation quality of the Blocks compiler. Exploiting aggressive data and instruction-level parallelisms would be your prime target. Which means you will be touching core stages of the backend - register allocation, scheduling, and MIR optimization stages. The exact scope of your thesis will be defined based on your interest and project goals.

The expected outcome of this MSc thesis is:

1. An extensive literature study on existing approaches for parallelism and energy-efficiency optimizations on the compiler
2. An evaluation of the most promising approaches using theoretical models and implementation of the selected approach on the compiler
3. A detailed evaluation of the implementation with a benchmark suite
4. A report and potential paper