Student assignment

Type: Graduation assignment
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Topic: investigation of multi-granular functional units on a coarse grained reconfigurable architecture.

Background:
At the electronic systems group we developed a very low-energy reconfigurable processor called Blocks. This processor outperforms a traditional microcontroller in performance with up to two orders of magnitude and typically uses approximately an order of magnitude lower energy to execute an application. Blocks achieves this by reconfiguring its hardware at runtime to match the properties of the application. If the application contains a lot of data parallelism then Blocks will be configured to form a vector processor, if there is instruction level parallelism then Blocks will form a VLIW processor. Anything in between, or even very application dependent structures (e.g. FFT or reduction trees) are also possible. By doing this cycles and memory accesses can be reduced significantly, leading to a much lower energy.

The data width required varies per application. Therefore, if we want to implement a general purpose energy efficient processor we would like to vary the width of the data-path. Blocks allows smaller width functional units to be connected to form a wider functional unit. However, we think this can be done much better than it is done now. Therefore this project will investigate possible improvements in this topic. In this project you will:

- Investigate the state of the art in multi-granular processing on CGRAs.
- Determine how multi-granular processing can be efficiently applied to Blocks.
- Investigate improvements to the state of the art of multi-granular processing on CGRAs by using the architectural properties of Blocks.
- Implement the most promising option(s) and verify your estimations.

If you are interested in this assignment, or have some questions, please come around to have a chat.