Mapping Convolutional Neural Networks on a Heterogeneous Multi-Core Platform

Assignment

Advances in camera sensor technology and computing platforms reduce camera cost and size, and increase computing performance, which together enables their usage in numerous applications. Popular examples include traffic monitoring systems as well as state-of-art wearable supports like Google glass. Recent work shows that Convolutional Neural Networks (CNNs) can outperform, and therefore replace, many algorithms for vision tasks. In a CNN, feature extraction and classification are combined in a single flexible model, and functionality can be adapted by simple weight updates.

In this project we will focus on the mapping of a novel CNN implementation for speed sign recognition. Related research indicates that these systems achieve better accuracy compared to single-stage hand crafted feature extraction. Figure 1 shows an example of such a CNN. 35 fps can be achieved with 720p HD video stream at an Nvidia GeForce GTX460 GPU. To reach acceptable performance on an energy efficient embedded platform which does not contain high-end processors, it is essential that parallelism and data reuse are well utilized.

The target platform we are going to map to is a heterogeneous multi-core platform consisting of: 1) a Network-on-Chip (NoC) subsystem with multiple Xentium DSP cores, memory tiles, DMA controller, and different interfaces; 2) a bus subsystem with LEON2 RISC processor and different peripherals. Figure 2 shows one example of this platform with two Xentium DSP cores. More Xentium DSP cores can be instantiated in the platform.
The assignment consists of four phases, including:

- **Algorithm & Background Learning:**
  - Study the provided CNN implementation and the corresponding documents;
  - Get to know the Xentium DSP core and how it is programmed;
  - Get to know Recore’s multi-core platform.

- **Single-Core Mapping:**
  - Mapping the provided CNN onto a single Xentium core;
  - Measure, evaluate, and optimize the performance.

- **Multi-core Platform Mapping:**
  - Mapping the provided CNN onto Recore’s multi-core platform;
  - Measure, evaluate, and optimize the performance.

- **Report Writing:**
  - Writing the internship report with findings and suggestions;
  - Presentation at Recore and TU/e.

**Requirements**

- Master student of Embedded System/Electrical Engineering
- Knowledge and experience of C and assembly
- Knowledge about DSP programming
- (Basic) knowledge about parallelism
Internship/Master Thesis Assignment

- Familiar with working under Linux system
- Well self-motivated

**Project Duration**

If as an internship project: 3~4 months
If as a master/thesis project: 8~9 months (more research topics will be added)

**Starting Time**

As soon as possible

**Allowance**

TBD (>500 euro)

**Location**

Recore Systems B.V.,
Capitool 5,
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The Netherlands

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**About Recore Systems B.V.**

Recore Systems is a fabless semiconductor company that develops advanced reconfigurable digital semiconductor IP. The company is specialized in reconfigurable multi-core designs that allow instant adaptation to new situations and offer a unique combination of flexibility, high performance, low power, and low cost. Scalability of the technology allows use in both consumer and high-end applications.

Recore's reconfigurable technology comprises reconfigurable DSP and NoC (Network-on-Chip) cores for multi- and many-core SoCs (System-on-Chips), design tools for easy integration in customer solutions and software libraries.