resource friendly SEU safe RISC-V MMU

Master thesis assignment

Background
RISC-V is a new instruction ISA that has promising features for both low-end as high-end applications. Technolution built its own RISC-V core targeting safety critical or security critical applications. These applications require the core to withstand or detect errors due to SEUs.

In order to make the entire path from the core to the memory safe for these errors we would like to have an MMU implementation that can detect (and possibly correct) SEU errors. Furthermore, we would like to add the MMU also for low-end applications. Therefore, the core needs to be scalable in the amount of resources used. Possibly only memory protection is performed for low-end applications.

The assignment
We want to develop a resource friendly MPU & MMU implementation that is protected for SEU errors. The MPU/MMU is written in VHDL and targeted for FPGAs.

Research questions
- What mechanisms are available to implement a MMU that has SEU protection in the data and control logic. Can both the control and data path use the same mechanisms for SEU protection or are different mechanisms more appropriate.
- Which architectural optimizations can be done to optimize the resource usage for the MMU/MPU when targeting low-end applications.

Activities
We have defined the following activities:
- Literature study of possible SEU detection and protection mechanisms.
- Literature study on resource friendly MMU implementations.
- Design an MMU architecture with the given constraints in mind.
- Implement the MMU/MPU preferably with parameters to optimize the resource usage versus number of supported processes, etc.
- Validate the design using automated tests.

Keywords
- MMU
- MPU
- VHDL
- RISC-V